Rectifying Properties of p-GaN Nanowires and an n-Silicon Heterojunction Vertical Diode

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ABSTRACT The heterojunction of a Pd-doped p-GaN nanowire and n-Si (100) is fabricated vertically by the vapor−liquid−solid method. The average diameter of the nanowire is 40 nm. The vertical junction reveals a significantly high rectification ratio of 10^3 at 5 V, a moderate ideality factor of ∼2, and a high breakdown voltage of ∼40 V. The charge transport across the p−n junction is dominated by the electron−hole recombination process. The voltage dependence of capacitance indicates a graded-type junction. The resistance of the junction decreases with an increase in the bias voltage confirmed by impedance measurements.

KEYWORDS: Heterojunction • rectification ratio • recombination • ideality factor • graded junction • breakdown voltage

1. INTRODUCTION

One-dimensional semiconductor nanostructures such as nanowires (NWs) and nanotubes are attractive for their morphology, size, and electronic properties compared to those of the bulk system. One-dimensional (1D) confinement of current carriers strongly influences the charge transport in nanowires. The nanoscale p−n junction is a fundamental unit in semiconductor nanotechnology. Semiconducting nanowires are very useful for constructing the one-dimensional p−n junction for novel nanoscale devices (1−8). GaN is a wide-band gap III−V compound semiconductor that makes it an excellent candidate for optoelectronic devices working at blue and near-ultraviolet wavelengths as well as high-temperature high-frequency electronics (9−13). The greatest advantage of GaN is the fact that both n-type and p-type forms can be synthesized by creating nitrogen and gallium vacancies, respectively. Moreover, p-type GaN can also be prepared by doping with divalent cation. Synthesis of perfectly aligned and assembly of semiconductor nanowires is an intriguing field of research.

Several techniques have been reported for manipulation of GaN nanowires into well-defined arrays for integrated devices. Lee et al. (14) have synthesized a high-brightness n-GaN nanowire diode on p-GaN using a dielectrophoresis method. One-dimensional GaN, nanostructure arrays with low defect density are fabricated employing porous anodic alumina films as the template and lead to high-performance devices (13). Dislocation free GaN nanowires have been grown on Si(111) by molecular beam epitaxy (15, 16). Zhong et al. (17) have synthesized GaN nanowires on sapphire by chemical vapor deposition. The metal−organic chemical vapor deposition method has been used to grow GaN nanowire arrays on $LiAlO_2$ and MgO (18). Tang et al. (19) have conducted controlled synthesis of a vertically aligned p-GaN nanorod array on an n-Si substrate by thermal evaporation of $GaCl_3$. Most of the earlier studies of the p−n junction are based on GaN nanorods with a diameter of ∼100 nm. Current−voltage characteristics deviate more from those of the ideal p−n junction. Nanowires are appropriate for the fabrication of the semiconductor nanoscale p−n junction. Further studies are required for large-scale integration, high-performance electronic devices, and understanding of junction properties.

A vast majority of semiconductor nanowires have been synthesized by the vapor−liquid−solid (VLS) mechanism, which makes use of a foreign element catalytic agent for NW nucleation and particular substrate for epitaxial growth. VLS offers a very low-cost method and size controllable growth of a semiconductor nanowire. Among the various substrates, the Si substrate may be promising for the heterojunction because of a reasonably large band gap difference between Si (1.1 eV) and GaN (3.4 eV). Here, we have fabricated a nitride-based p−n junction heterostructure consisting of phosphorus-doped n-type Si(100) and divalent Pd-doped p-type GaN NWs. The systematic investigation of their transport properties may open the possibility of GaN nanowire-based optoelectronic devices.

2. EXPERIMENTAL SECTION

Palladium-doped GaN NWs were prepared via the metal (Au)-catalyzed vapor−liquid−solid (VLS) method using ammonia (99.99%, Matheson), gallium metal (99.99%, Aldrich), and palladium chloride ($PdCl_2$) as the N, Ga, and Pd sources, respectively. Phosphorus-doped n-type Si(100) was used as the growth substrate. At first, the bulk GaN precursor was prepared by dissolving gallium metal in a 69% HNO_3 (Aldrich) solution such that the Ga:HNO_3 molar ratio was greater than 1:3 under ultrasonication. The solution was then diluted when it was added to 2-propanol under stirring such that the Ga:2-propanol molar ratio was 1:90 and allowed to stir for 30 min. A white precipitate was obtained upon slow addition of 25% NH_4OH (ammonia solution) to this solution under vigorous stirring, which was separated by centrifugation, washed in ethanol, and dried at 60 °C for 24 h. Nitridation was conducted in an alumina boat kept in a quartz tube with an inner diameter equal to 24 mm under an ammonia flow. The tube was flushed with

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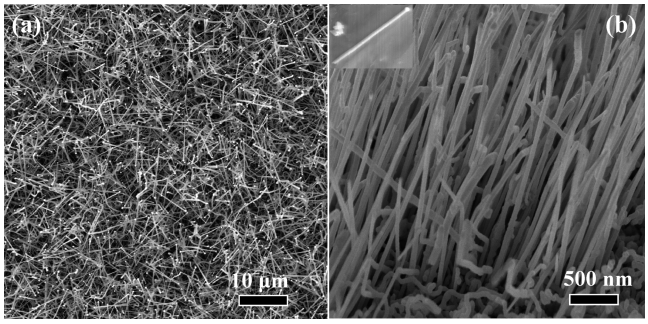

FIGURE 1. (a) FE-SEM image of Pd-doped GaN nanowires at a low magnification. (b) High-magnification image. The inset shows a single nanowire.

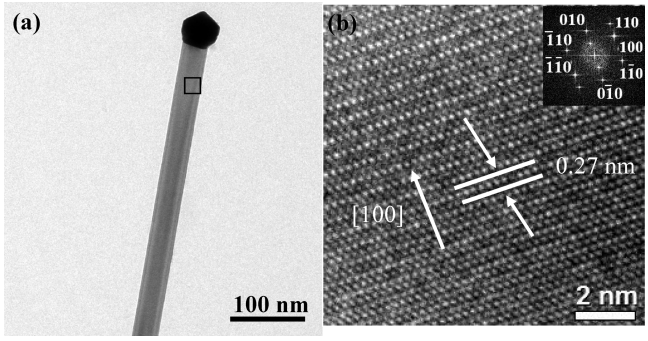

FIGURE 2. (a) TEM image of a single 40 nm diameter Pd-doped GaN nanowire that terminates in a faceted nanoparticle of higher contrast. (b) HRTEM image of the same nanowire. The inset shows a FFT pattern of HRTEM image.

nitrogen for 30−45 min; ammonia was allowed to flow into the tube at a rate of 200 sccm, and the temperature was fixed at 900 °C for 60 min. A yellow-colored pure GaN bulk powder was obtained. The GaN powder and $PdCl_2$ were taken as the source material. GaN bulk powder and $PdCl_2$ powders were placed separately in two alumina boats, which were loaded inside a quartz tube reactor. A silicon substrate, on which a 3−5 nm thick Au film was deposited, was positioned 10 cm from the GaN source. Ammonia was allowed to flow at a rate of 300 sccm while the temperature was increased and decreased. The temperatures of GaN, the $PdCl_2$ source, and the substrate were set at ∼1100, ∼900, and ∼850 °C, respectively. The Pd content was controlled via adjustment of the evaporation temperature of $PdCl_2$. Argon gas was continuously passed at a rate of 500 sccm for 60 min during the synthesis. All characterization details are provided in the Supporting Information.

3. RESULTS AND DISCUSSION

The high-resolution X-ray diffraction (XRD) pattern of the Pd-doped GaN NWs (Figure S1 of the Supporting Information) indicates the wurtzite crystalline structure of GaN (JCPDS Card 50-0792). Samples are highly crystalline in nature in the absence of other phases. Panels a and b of Figure 1 show the low- and high-magnification SEM micrographs, respectively, of the high-density Pd-doped GaN NWs grown on the n-type Si substrate. The inset of Figure 1b shows a single Pd-doped GaN NW. The straight nanowires were grown at 1100 °C using thermal vapor transport of a $GaN/PdCl_2/NH_3$ mixture. The growth mechanism of the nanowires follows the vapor−liquid−solid (VLS) mechanism using the Au catalytic nanoparticles. The Pd content was controlled via adjustment of the evaporation temperature of $PdCl_2$. The transmission electron microscope image of a single nanowire is shown in Figure 2a. The Au catalytic nanoparticle at the tip of the single nanowire provides the evidence of VLS growth. The transmission electron microscopy (TEM) image explicitly reveals their smooth surface, average diameter of 40 nm, and length of 30−40 μm. The lattice-resolved TEM image and corresponding fast Fourier transform electron diffraction (FFT ED) pattern of a selected nanowire reveal that it is composed of single-crystalline wurtzite-structured GaN (Figure 2, panel b and inset). It shows spacing between neighboring (100) planes of ∼0.27 nm (JCPDS Card 50-0792). The FFT ED pattern generated from the inversion of the TEM image using Digital Micrograph GMS1.2 (Gatan Inc.) at the [001] zone axis confirms that it has the [100] growth direction. Energy dispersive spectroscopy (EDS) analysis indicates that the Pd content of the individual nanowire is to be ∼1.50%, with a homogeneous distribution being observed over the whole nanowire. The average value was obtained from the EDS measurements of four to eight nanowires. No other impurities were observed in nanowires. The Ga:N atomic ratio is approximately 1:0.82. The content of dopant Pd was also verified via inductively coupled plasma atomic emission spectroscopy (ICP-AES) very accurately, with an average Pd content of 1.46% (see Figure S2 of the Supporting Information).

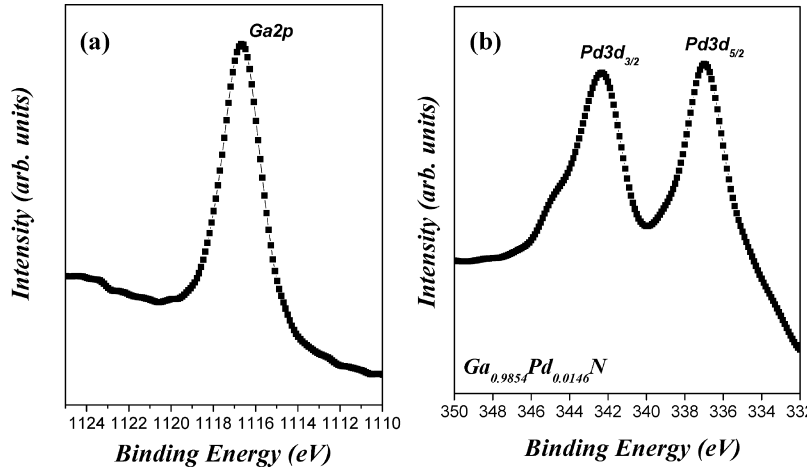

FIGURE 3. (a) Ga2p and (b) Pd 3d core level X-ray photoelectron spectra of Pd-doped GaN nanowires.

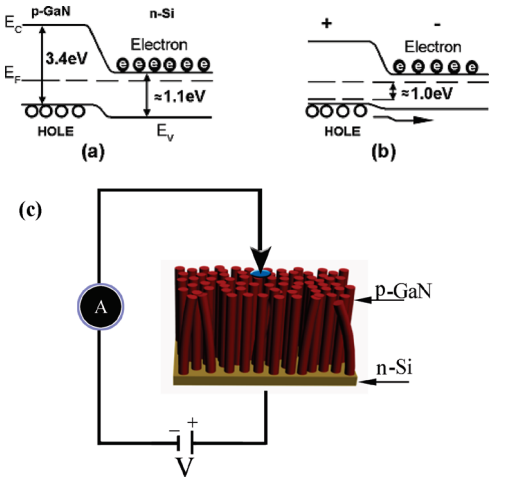

FIGURE 4. Energy diagram with respect to vacuum level (a) before biasing and (b) after forward biasing. (c) Schematic of the device structure at reversed bias.

The valence states of Ga and Pd in doped GaN nanowires were determined by X-ray photoelectron spectroscopy (XPS). The Ga 2p and Pd 3d core level spectra are shown in Figure 3, confirming the valence state of the Ga and Pd. Figure 3a shows the fine-scanned Ga $2p_{3/2}$ peak appears at 1116.7 eV. Figure 3b corresponds to the finely scanned Pd $3d_{3/2}$ (337 eV) and Pd $3d_{5/2}$ (342.3 eV) peaks of the Pd-doped GaN nanowires. This confirms that Ga is in the +3 state and Pd is in the +2 state. A shift in the Ga peak is also observed, suggesting that, in p-type GaN, a process for the transfer of a shallow acceptor's hole onto Pd^{2+} to form Pd^{3+}, in which the Pd^{3+} ions act as effective shallow donors, exists. This hole transfer can be described as $Pd^{2+} + h^+$ (acceptor) → Pd^{3+}. This also shows that Pd is incorporated into the GaN lattice. The carrier concentration and conductive type of these Pd-doped GaN nanowires were determined by Hall measurements at room temperature by the van der Pauw method. The carrier concentration of Pd-doped p-type GaN nanowires is 3.0×10^{18} cm^{-3} with a mobility of 118 cm^2 V^{-1} s^{-1}. The valence state of Pd and p-type behavior clearly indicate that divalent Pd replaces trivalent Ga in the doped GaN nanowires.

The device structure consisting of nanowires is shown in Figure 4c. In this device, gold (Au) metal is chosen as the bottom and top electrodes for electrical characterization. In the VLS process, Au deposited on Si substrate acts as the catalyst. Au makes an alloy with GaN at the tip of each nanowire, as confirmed by the HRTEM image shown in Figure 2b. Experimentally, it is found that the formation of alloy with Au does not show a Schottky barrier between Au and p-type GaN (20, 21). To check the ohmic contact between Au and Si substrate, we measured the current density−voltage (I−V) characteristics of the Au−Si−Au system. The I−V curve reveals linear behavior (see Figure S4 of the Supporting Information), confirming an ohmic contact. The resistance calculated from the I−V plot is 13.05 $\times 10^{-2}$ Ω cm^{-2}, which is negligibly small with respect to substrate. Figure 5a shows the current density−voltage (I−V) characteristics of the Au−p-GaN−n-Si−Au device. The fabricated heterojunction exhibits a clear rectifying type of

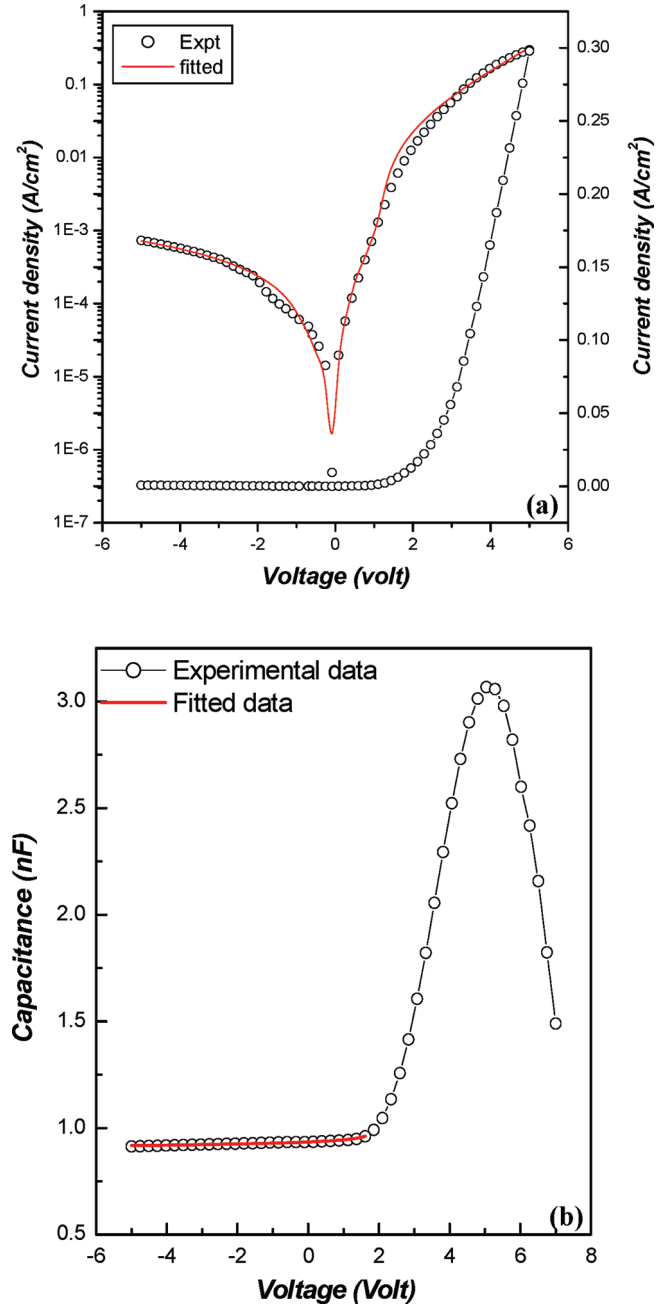

FIGURE 5. (a) Current density−voltage (I−V) and (b) capacitance−voltage (C−V) relationships of a typical diode.

behavior. Under forward bias, an obvious turn-on voltage is observed at ~1.2 V. The forward current density (I_F) of the junction at 5 V is 318 mA/cm^2, while the reverse leakage current density (I_R) at −5 V bias is less than 0.7 mA/cm^2. The rectification ratio (I_F/I_R) is greater than 10^3 at ±5 V, considerably higher than that previously reported for the GaN-Si diode (15). A high rectification ratio implies a good p−n junction between the p-type GaN and n-type Si(100) substrate. The breakdown voltage of the present diode is 40 V, 50 times higher than the threshold voltage.

The forward bias has been analyzed using the thermo ionic emission model and the reverse bias by the reverse soft breakdown model (22). The total current is

$$I = I_s[\exp(qV/\eta kT) - 1] - I_{tun}[\exp(qV/\eta_{tun}kT) - 1] \quad (1)$$

where I_s and I_{tun} are the reverse saturation current and tunneling saturation current, respectively, and η and η_{tun} are the ideality factor and tunneling ideality factor, respectively. The first and second terms of eq 1 represent the forward current and reverse current, respectively. The η value of 1 corresponds to diffusion, and the η value of 2 corresponds to electron−hole recombination. The best-fitted values of η and η_{tun} are 1.99 and 0.98, respectively. The calculated η value of 1.99 suggests an electron−hole recombination process in electric conduction. Recombination occurs because of the presence of a large minority carrier. The surface pinning of the Fermi level leads to the depletion of the charge carrier, which gives rise to recombination at the surface (13). A large surface area of nanowires leads to prominent surface recombination.

Figure 4a shows the schematic energy band diagram of a p-GaN−n-Si junction at equilibrium. The barrier at the p−n junction arises because of the band offsets of p-GaN and n-Si semiconductors. The barrier potential also depends on the nature of the interface between two semiconductors. An application of external voltage modifies the electrostatic barrier and interband separation. Forward bias lowers the potential barrier across the junction because of the closer approaches of energy bands as shown in Figure 4b. This enhances the flow of current through the junction. The potential barrier becomes larger for reverse bias, which slows the flow of current.

Nanowires have a diameter of 40 nm and a length of 30−40 μm. The p−n junction on the Si(100) substrate is relatively smaller than the junction formed by GaN nanorods. The most interesting observation is that the ideality factor is significantly lower than that of the nanorod-based p−n junction. A higher ideality factor commonly arises because of the formation of electrically active states in the space charge region. The lower value of the ideality factor manifests the absence of defects in the p−n junction. In the VLS process, the formation of such states in the p−n junction area may be less probable. Thus, the improvement of junction characteristics has been realized compared to those of the Mg-doped p-GaN nanorod arrays (19, 23).

The distributions of donors and acceptors across the p−n junction influence the characteristic behavior of the depletion layer. The nature of the p−n junction, i.e., abrupt or graded junction, can be understood from the capacitance−voltage ($C-V$) relationship. We have studied $C-V$ relationship at a 100 kHz frequency for the Au−n-Si−p-GaN−Au heterojunction as shown in Figure 5b. Under reverse bias, capacitance decreases as the absolute value of the applied voltage increases, because of the increase in the width of the depletion region. The reverse bias behavior of the $C-V$ relationship is typical of a reverse biased p−n junction. The depletion capacitance provides evidence of the formation of a depletion region due to the p−n junction formed by n-GaN and p-Si (24). This p−n junction capacitance can also been fitted by the expression

$$C = C_0/(1 - V/V_0)^m \quad (2)$$

where C_0 represents the zero bias junction capacitance and m is the grading coefficient. The fitting parameters C_0 and m were found to equal 9.31×10^{-10} F and 0.013, respectively. In the case of the abrupt junction, the value of m is 0.5. The smaller value of m indicates the p−n junction is a graded junction. The p−n junction is fabricated at 900 °C for 60 min. Thermal diffusion of acceptors into the n-type region and donors into the p-type region yields a distribution of impurities in the depletion region. As a result, a graded junction is formed instead of an abrupt junction. The estimated junction potential V_0 is 1.85 V.

Under a forward bias lower than 4.5 V, capacitance increases with the applied voltage. When forward bias increases more, capacitance increases exponentially, which has been observed previously (25), and above 5 V, capacitance sharply decreases. This is probably an effect of the free carriers, which are stored in the depletion region of the p−n junction. At very large forward bias, the junction barrier height is lower than the thermal voltage and the energy distribution of the free carriers in the space charge region is such that the junction barrier is nearly transparent to the sizable majority carrier population on both sides of the region. As a result, capacitance decreases abruptly with an increase in forward biasing voltage.

We have investigated the impedance spectroscopy of the Au−Si−GaN−Au system within the frequency (ω) range from 5 Hz to 10 MHz to gain information about charge transfer and charge accumulation inside the device. Real part Re(Z) and imaginary part Im(Z) of the complex impedance $Z(\omega)$ [where $Z(\omega) = \mathrm{Re}(Z) + j \times \mathrm{Im}(Z)$] have been measured using the dependence of bias voltage. The detailed device impedance variation with respect to frequency at different DC bias values (V_{DC}) has been described by a Cole−Cole plot as depicted in Figure 6. An almost ideal semicircle has been obtained for the Re(Z) versus Im(Z) plot at bias voltages of 1.0, 1.5, and 2.0 V, indicating that the device can be represented by an equivalent parallel $R-C$ circuit (26) in which the capacitance (C) and resistance (R) are frequency-independent parameters. Figure 5 also shows that the variation of Im(Z) for V_{DC} values of 0 and 0.5 V in a low frequency range is very sharp and does not follow a complete semicircle, which indicates that in this DC bias range the diode behaves like a pure capacitor. From Figure 6, it is very clear that the value of R sharply decreases when V_{DC} increases from 1.0 to 2 V, which is very obvious because of the diode's gradually increasing conductance above the turn-on voltage. These data are also consistent with the $I-V$ curve (Figure 5a), which indicates that the turn-on voltage is 1.2 V. From Figure 6, it is also clear that all impedance curves begin at the origin of the Re(Z) versus Im(Z) plot, not from any finite positive Re(Z) value, which indicates the negligible

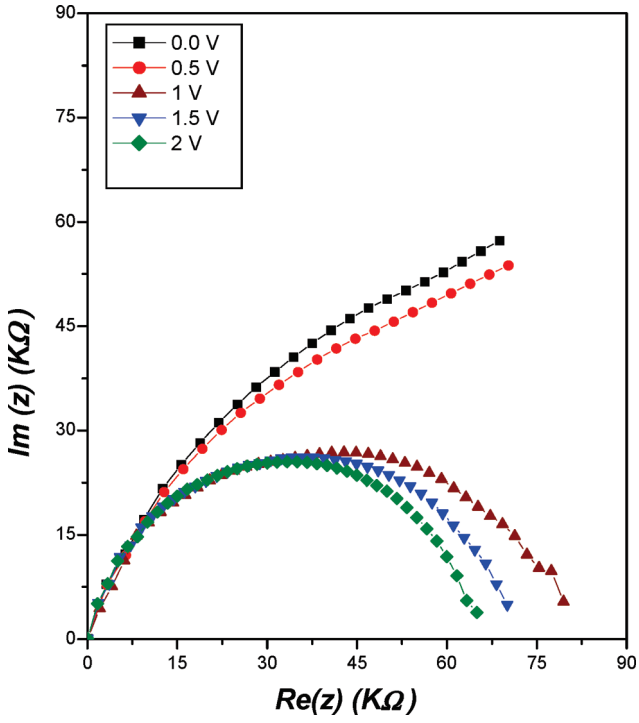

FIGURE 6. Cole–Cole [complex impedance Re(Z) vs Im(Z)] plot at different DC bias voltages (V_{DC}).

contribution of probe resistance and capacitance relative to the whole device.

4. CONCLUSIONS

Current–voltage relationships reveal that Pd-doped GaN nanowires grown on n-type Si(100) are p-type semiconductors. Vertically aligned diodes exhibit excellent current rectifying behavior with an ideality factor of ~2. A low ideality factor suggests a defect free p–n junction formed by the nanowire in the vapor–liquid process. The reverse breakdown voltage of the present nanowire p–n junction is substantially high (~40 V). Capacitance–voltage relationships indicate that the junction is a graded junction. The high rectification ratio, low ideality factor, and high breakdown voltage make this junction suitable for device application.

Supporting Information Available: All characterization details like X-ray diffraction (XRD), EDS spectra, current voltage (I–V) relationships, Hall measurements, and details of materials used and specifications of instruments used. This material is available free of charge via the Internet at http://pubs.acs.org.

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